IMPROVED BALL GRID ARRAY PACKAGE AND PROCESS FOR MANUFACTURING SAME

FIELD OF THE INVENTION

[0001] The present invention relates in general to integrated circuit packaging, and in particular to an improved ball grid array package with enhanced thermal characteristics and a unique method of manufacturing.

BACKGROUND OF THE INVENTION

[0002] High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by industry demands for increased thermal and electrical performance and decreased size and cost of manufacture.

[0003] In general, array packaging such as Plastic Ball Grid Array (PBGA) packages provide a high density of interconnects relative to the surface area of the package. However, typical PBGA packages include a convoluted signal path, giving rise to high impedance and an inefficient thermal path which results in low thermal dissipation performance. With increasing package density, the spreading of heat generated by the package is increasingly important.

[0004] Reference is made to Figure 1, which shows an elevation view of a conventional PBGA package indicated generally by the numeral 20. The PBGA package 20 includes a substrate 22 and a semiconductor die 24 attached to the substrate 22 by a die adhesive. Gold wire bonds 26 electrically connect the die 24 to metal traces on the substrate 22. The wire bonds 26 and die 24 are encapsulated in an overmold material 28. A ball grid array 30, in the form of solder bumps, is disposed on the bottom surface of the substrate 22 for signal transfer. Because of the absence of a thermal path away from the semiconductor die 24, thermal dissipation in this package is poor.

[0005] Variations to conventional BGA packages have been proposed for the purpose of increasing thermal and electrical performance. One particular variation includes the addition of a metal heat spreader to the package, as shown in Figure 2 which shows an elevation view of a PBGA package 20 of the prior art including the heat spreader indicated by the numeral 32. In general, the metal heat spreader 32 is fixed to the molded package. This package suffers disadvantages, however, as heat must be dissipated from the semiconductor die 24, through the

molding compound 28 and then through the heat spreader 32. Furthermore, this package is not suitable for package stacking which is desirable for decreasing motherboard area that is used when the packages are mounted thereon.

[0006] It is therefore an object of an aspect of the present invention to provide a process for manufacturing a BGA package that obviates or mitigates at least some of the disadvantages of the prior art.

SUMMARY OF THE INVENTION

[0007] In one aspect, a process for manufacturing an integrated circuit package is provided. The process includes forming a plurality of solder balls on a first surface of a substrate and mounting a semiconductor die to the substrate such that bumps of the semiconductor die are electrically connected to conductive traces of the substrate. The semiconductor die and the solder balls are encapsulated in an overmold material on the substrate such that portions of the solder balls are exposed. A ball grid array is formed such that bumps of the ball grid array are electrically connected to the conductive traces and the integrated circuit package is singulated.

[0008] In another aspect, an integrated circuit package is provided. The package includes a substrate having a plurality of conductive traces and a plurality of solder balls disposed on a first surface of the substrate. A semiconductor die is mounted to the substrate such that bumps of the semiconductor die are electrically connected to conductive traces of the substrate. An overmold material encapsulates the semiconductor die and the solder balls on the substrate such that portions of the solder balls are exposed. A ball grid array is in electrical connection with the conductive traces.

[0009] Advantageously, solder balls are embedded in the overmold material. The solder balls provide a heat path for heat dissipation from the package. Also, the solder balls in the overmold material enable package stacking which provides for reduced mother board area when the packages are in use and improves package to package communication signal paths.

[0010] In another aspect, bumps of a ball grid array are mounted on solder balls which are encapsulated in overmold material. This package provides better control of solder ball stand off clearance than prior art packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 is an elevation view of a conventional plastic ball grid array package;

[0012] Figure 2 is an elevation view of a prior art plastic ball grid array package including a heat spreader;

[0013] Figures 3A to 3G show processing steps for manufacturing a ball grid array package in accordance with one embodiment of the present invention;

[0014] Figure 4 is a top plan view of the individual BGA package shown in Figure 3G;

[0015] Figure 5 is a side elevation view of the BGA package of Figure 3G stacked with another BGA package;

[0016] Figures 6A to 6I show processing steps for manufacturing a ball grid array package in accordance with another embodiment of the present invention;

[0017] Figures 7A to 7G show processing steps for manufacturing a ball grid array package in accordance with another embodiment of the present invention;

[0018] Figures 8A to 8H show processing steps for manufacturing a ball grid array package in accordance with still another embodiment of the present invention;

[0019] Figures 9A to 9I show processing steps for manufacturing a ball grid array package in accordance with yet another embodiment of the present invention; and

[0020] Figures 10A to 10G show processing steps for manufacturing a ball grid array package in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Reference is now made to Figures 3A to 3G to describe a process for manufacturing a ball grid array integrated circuit package, referred to herein as a ball grid array package, according to one embodiment of the present invention. To simplify the description, the numerals used previously in describing Figure 1 will be used again after raising the numerals by 100 where parts to be described correspond to parts already described.

[0022] Referring to Figure 3G, the ball grid array (BGA) package is indicated generally by the numeral 120 and includes a substrate 122 having a plurality of conductive traces and a

plurality of solder balls 134 disposed on a first surface of the substrate 122. A semiconductor die 124 is mounted to the substrate 122 such that bumps of the semiconductor die 124 are electrically connected to the conductive traces of the substrate 122. An overmold material 128 encapsulates the semiconductor die 124 and the solder balls 134 on the substrate 122 such that portions of the solder balls 134 are exposed. A ball grid array 130 is electrically connected with the conductive traces of the substrate 122.

[0023] The process for manufacturing the ball grid array package 120, according to one embodiment of the present invention, will now be described in more detail. Referring to Figure 3A, the substrate 122, a BT resin/glass epoxy printed circuit board with conductive traces for signal transfer is shown. A solder mask is disposed on the lower surface of the substrate with portions of the conductive traces, also referred to as interconnects, exposed. The substrate 122 is in the form of an array strip for producing a number of BGA units. Three such units are depicted in an array in Figure 3A, however, the process is herein described with reference to a single unit.

[0024] The plurality of solder balls 134 are formed on solder ball pads on the upper surface of the substrate 122 using conventional positioning techniques (Figure 3B). To attach the solder balls 134, a flux is added to the solder balls 134 prior to placement and, after placement the solder balls 134 are reflowed using known reflow techniques. The solder balls 134 are thereby connected to the solder ball pads of the substrate 122.

[0025] A singulated semiconductor die 124 is conventionally mounted to the upper surface of the substrate 122 using a suitable die attach technique, such as attachment using a die attach epoxy adhesive and curing of the epoxy (Figure 3C). It will now be understood that the solder balls 134 are located around the periphery of the semiconductor die 124.

[0026] The semiconductor die 124 has a conductive pad array formed thereon and wire bonds 126 are bonded between bumps of the conductive pad array of the semiconductor die 124 and the conductive traces of the substrate 122 using conventional wire bonding techniques (Figure 3D). The semiconductor die 124 is thereby electrically connected to the conductive traces of the substrate 122.

[0027] Encapsulation in the overmold material 128 follows. The semiconductor die 124 and the solder balls 134 are encapsulated in the overmold material 128 by molding in a mold die such that portions of the solder balls 134 that are distal the substrate 122, are exposed. The

solder balls 134 are deformed into substantially spheroidal shapes during molding as a result of pressure from the surface of the mold die (Figure 3E).

[0028] Next, a ball grid array 130 in the form of solder bumps, is formed on the lower surface of the substrate 122 by conventional positioning (Figure 3F). To attach the solder bumps of the ball grid array 130, a flux is added to the solder prior to placement and, after placement, the solder is reflowed using known reflow techniques. The solder bumps of the ball grid array 130 are thereby connected to the conductive traces of the substrate 122 and through the wire bonds 126 to the semiconductor die 124. The ball grid array 134 provides signal and power connections as well as ground connections for the semiconductor die 124.

[0029] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 3G. Thus, the individual BGA package 120 is isolated from the strip. Figure 4 shows a top plan view of the individual BGA package shown in Figure 3G.

[0030] The BGA package 120 produced by this process is particularly suitable for stacking with other BGA packages, as shown in Figure 5

[0031] Reference is now made to Figures 6A to 6I to describe a process for manufacturing the ball grid array package 120 in accordance with an alternative embodiment of the present invention. Figures 6A to 6C are similar to Figures 3A to 3C and therefore need not be further described herein. In Figure 6D, however, a die adapter 136 is mounted to the semiconductor die 124 using a thermally conductive adhesive for conducting heat from the semiconductor die 124 to the die adapter 136. In the present embodiment, the die adapter 136 is copper, however other suitable materials can be used, as will occur to those skilled in the art.

[0032] Figures 6E to 6H are similar to Figures 3D to 3G and therefore need not be further described herein. As shown in Figure 6I, an external heat sink 138 is then mounted to the package using, for example, a thermally conductive adhesive. Alternatively, the heat sink 138 is soldered to the exposed portions of the solder balls 134. Thus, a heat transfer path is provided through the solder balls 134 to the heat sink 138. The use of a die adapter 136 further improves heat transfer away from the semiconductor die 124.

[0033] Reference is now made to Figures 7A to 7G to describe a process for manufacturing a ball grid array package 120 in accordance with another embodiment of the present invention. Referring to Figure 7A, the substrate 122 of a polyimide tape is shown. The substrate 122

includes a metal layer on both the top side and the bottom side. The metal layer on the top side acts as a heat spreader for dispersing heat while the metal layer on the bottom side includes a circuit pattern of conductive traces for signal transfer. The substrate 122 is in the form of an array strip for producing a number of BGA units. Two such units are depicted in the array in Figure 7A.

[0034] A plurality of solder balls 134 are formed on solder ball pads on the lower surface of the substrate 122 using conventional positioning techniques (Figure 7B). To attach the solder balls 134, a flux is added to the solder balls 134 prior to placement and, after placement the solder balls 134 are reflowed using known reflow techniques. The solder balls 134 are thereby connected to the solder ball pads of the substrate 122 which are electrically connected to the conductive traces of the substrate 122.

[0035] A singulated semiconductor die 124 is conventionally mounted to the lower surface of the substrate 122 using a suitable die attach technique, such as attachment using a die attach epoxy adhesive and curing of the epoxy (Figure 7C). It will now be understood that the solder balls 134 are located around the periphery of the semiconductor die 124.

[0036] The semiconductor die 124 has a conductive pad array formed thereon and wire bonds 126 are bonded between bumps of the conductive pad array of the semiconductor die 124 and the conductive traces of the substrate 122 using conventional wire bonding techniques (Figure 7D). The semiconductor die 124 is thereby electrically connected to the conductive traces of the substrate 122.

[0037] Encapsulation in the overmold material 128 follows. The semiconductor die 124 and the solder balls 134 are encapsulated in the overmold material 128 by molding in a mold die such that portions of the solder balls 134 that are distal the substrate 122, are exposed. The solder balls 134 are deformed into substantially spheroidal shapes during molding as a result of pressure from the surface of the mold die (Figure 7E).

[0038] Next, a ball grid array 130 in the form of solder bumps, is formed on the exposed portions of the solder balls 134 by conventional positioning (Figure 7F). To attach the solder bumps of the ball grid array 130, a flux is added to the solder prior to placement and, after placement, the solder is reflowed using known reflow techniques. The solder bumps of the ball grid array 130 are thereby connected to the conductive traces of the substrate 122 and through the wire bonds 126 to the semiconductor die 124. The ball grid array 134 provides signal and

power connections as well as ground connections for the semiconductor die 124.

[0039] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 7G. Thus, the individual BGA package 120 is isolated from the strip.

[0040] Reference is now made to Figures 8A to 8H to describe a process for manufacturing a ball grid array package 120 in accordance with still another embodiment of the present invention. Referring to Figure 8A, the substrate 122 of a polyimide tape is shown. The substrate 122 includes a metal layer on the bottom side thereof which includes a circuit pattern of conductive traces for signal transfer. A cavity extends through the substrate 122. It will be understood that the substrate 122 is in the form of an array strip for producing a number of BGA units. Two such units are depicted in an array in Figure 8A, however, the process is herein described with reference to a single unit.

[0041] The substrate is laminated to a metal strip 140 which acts as a heat spreader for dispersing heat (Figure 8B).

[0042] A plurality of solder balls 134 are formed on solder ball pads on the exposed lower surface of the substrate 122 using conventional positioning techniques (Figure 8C). To attach the solder balls 134, a flux is added to the solder balls 134 prior to placement and, after placement the solder balls 134 are reflowed using known reflow techniques. The solder balls 134 are thereby connected to the solder ball pads of the substrate 122 which are electrically connected to the conductive traces of the substrate 122.

[0043] A singulated semiconductor die 124 is mounted to the metal strip 140 which is laminated to the substrate 122, using a suitable die attach technique. Thus, the semiconductor die 124 is attached to the substrate 122 via the metal strip 140 (Figure 8D). It will now be understood that the solder balls 134 are located around the periphery of the semiconductor die 124.

[0044] The semiconductor die 124 has a conductive pad array formed thereon and wire bonds 126 are bonded between bumps of the conductive pad array of the semiconductor die 124 and the conductive traces of the substrate 122 using conventional wire bonding techniques (Figure 8E). The semiconductor die 124 is thereby electrically connected to the conductive traces of the substrate 122.

[0045] Encapsulation in the overmold material 128 follows. The semiconductor die 124 and

the solder balls 134 are encapsulated in the overmold material 128 by molding in a mold die such that portions of the solder balls 134 that are distal the substrate 122, are exposed. The solder balls 134 are deformed into substantially spheroidal shapes during molding as a result of pressure from the surface of the mold die (Figure 8F).

[0046] Next, a ball grid array 130 in the form of solder bumps, is formed on the exposed portions of the solder balls 134 by conventional positioning (Figure 8G). To attach the solder bumps of the ball grid array 130, a flux is added to the solder prior to placement and, after placement, the solder is reflowed using known reflow techniques. The solder bumps of the ball grid array 130 are thereby connected to the conductive traces of the substrate 122 and through the wire bonds 126 to the semiconductor die 124. The ball grid array 134 provides signal and power connections as well as ground connections for the semiconductor die 124.

[0047] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 8H. Thus, the individual BGA package 120 is isolated from the strip.

[0048] Reference is now made to Figures 9A to 9I to describe a process for manufacturing a ball grid array package 120 in accordance with yet another embodiment of the present invention. Referring to Figure 8A, the substrate 122 of a polyimide tape is shown. The substrate 122 includes a metal layer on the bottom side thereof which includes a circuit pattern of conductive traces for signal transfer. A cavity extends through the substrate 122 and a plurality of smaller holes also extend through the substrate. It will be understood that the substrate 122 is in the form of an array strip for producing a number of BGA units. Two such units are depicted in an array in Figure 8A, however, the process is herein described with reference to a single unit.

[0049] The substrate is laminated to a metal strip 140 that is preplated with suitable metal for ground bonding. Such metal plating includes, for example silver, nickel followed by gold and nickel followed by palladium (Figure 9B).

[0050] Solder is then applied to the holes of the substrate and the solder is reflowed, followed by a flattening process such as coining to result in a substantially flat surface (Figure 9C).

[0051] A plurality of solder balls 134 are formed on solder ball pads on the exposed lower surface of the substrate 122 and on the solder in the holes of the substrate 122, using

conventional positioning techniques (Figure 9D). To attach the solder balls 134, a flux is added to the solder balls 134 prior to placement and, after placement the solder balls 134 are reflowed using known reflow techniques. Thus, some of the solder balls 134 are connected to the solder ball pads of the substrate 122 which are electrically connected to the conductive traces of the substrate 122. Others of the solder balls are connected to the metal strip 140.

[0052] A singulated semiconductor die 124 is mounted to the metal strip 140 which is laminated to the substrate 122, using a suitable die attach technique. Thus, the semiconductor die 124 is attached to the substrate 122 via the metal strip 140 (Figure 9E). It will now be understood that the solder balls 134 are located around the periphery of the semiconductor die 124.

[0053] The semiconductor die 124 has a conductive pad array formed thereon and wire bonds 126 are bonded between bumps of the conductive pad array of the semiconductor die 124 and the conductive traces of the substrate 122 using conventional wire bonding techniques (Figure 9F). The semiconductor die 124 is thereby electrically connected to the conductive traces of the substrate 122.

[0054] Encapsulation in the overmold material 128 follows. The semiconductor die 124 and the solder balls 134 are encapsulated in the overmold material 128 by molding in a mold die such that portions of the solder balls 134 that are distal the substrate 122, are exposed. The solder balls 134 are deformed into substantially spheroidal shapes during molding as a result of pressure from the surface of the mold die (Figure 9G).

[0055] Next, a ball grid array 130 in the form of solder bumps, is formed on the exposed portions of the solder balls 134 by conventional positioning (Figure 9H). To attach the solder bumps of the ball grid array 130, a flux is added to the solder prior to placement and, after placement, the solder is reflowed using known reflow techniques. Some of the solder bumps of the ball grid array 130 are thereby connected to the conductive traces of the substrate 122 and through the wire bonds 126 to the semiconductor die 124. Other solder bumps of the ball grid array 130 are connected to the metal strip 140. Thus, the solder bumps provide signal and power connections as well as ground connections for the semiconductor die 124.

[0056] Singulation of the individual BGA unit from the array strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 9I. Thus, the individual BGA package 120 is isolated from the strip.

[0057] Figures 10A to 10G show processing steps for manufacturing a ball grid array package 120 in accordance with another embodiment of the present invention. Figures 10A and 10B are similar to Figures 3A and 3B and therefore need not be further described herein. In Figure 10C, however, the semiconductor die 124 is mounted in a flip-chip orientation on the substrate 122. The semiconductor die 124 is mounted to the substrate 122 by solder ball connections 138 between pads of the semiconductor die 124 with interconnect pads of the substrate 122, using known pick and place technique.

[0058] Next, the area under the semiconductor die 124 is filled with a thermosetting plastic compound, referred to generally as an underfill material 132. The underfill material 132 surrounds the solder ball connections 138 that connect the semiconductor die 124 and the interconnect pads of the substrate 122 (Figure 10D).

[0059] Figures 10E to 10G are similar to Figures 3E to 3G and therefore need not be further described herein.

[0060] Alternative embodiments and variations are possible. For example, the packages described herein have been described as being polyimide and BT resin/glass epoxy printed circuit board substrates. However, other substrates may be used such as ceramic substrates and organic laminates. Also, the size and shape of many of the elements described and shown can vary. Still other embodiments and variations may occur to those skilled in the art. All such embodiments and variations are believed to be within the scope and sphere of the present invention.